ABSTRACT OF THE DISCLOSURE

A data storage device having parallel memory planes is disclosed. Each memory plane includes a first resistive cross point plane of memory cells, a second resistive cross point plane of memory cells, a plurality of conductive word lines shared between the first and second planes of memory cells, a plurality of bit lines, each bit line coupling one or more cells from the first plane to another memory cell in the second plane, and a plurality of unidirectional elements. Further, the one unidirectional element couples a first memory cell from the first plane to a selected word line and a selected bit line in a first conductive direction and a second unidirectional element couples a second cell from the second plane to the selected word line and selected bit line in a second conductive direction. The device further provides for a unidirectional conductive path to form from a memory cell in the first plane to a memory cell in the second plane sharing the same bit line.